REMARKS

This application has been reviewed in light of the Final Office Action mailed July 12, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-9 are pending in the application with Claim 1 being in independent form. By the present amendment, Claims 1 and 3 have been amended. No new subject matter has been introduced by way of the present amendment.

Firstly, while reviewing the application in connection with this Office Action, an error was found in the specification. Specifically, paragraph 0011 recites: "...usually on the other of two or three times larger..." but should, instead, recite: "...usually on the order of two or three times larger..." (Emphasis added). Accordingly, a replacement paragraph has been submitted by way of the present amendment. (See: "Amendments to the Specification" of the present response).

I. Rejection of Claims 1-9 Under 35 U.S.C. §112, Second Paragraph

Claims 1-9 have been rejected under 35 U.S.C. §112, second paragraph for allegedly being indefinite. Specifically, the Examiner alleges that Claim 1 does not clearly define the exact structure of the claimed device, such that the inventive structure is not clear as to the relative dimensions of the N and P-type transistors in each of the inverters of the invention. Additionally, the Examiner alleges that the limitation recited by Claim 3, stating that the gate width of the first transistor is set so that a change in the edge flank is slowed down, is vague as to the actual structure of the transistor. In response, Claims 1 and 3 have been amended in a manner believed to obviate the rejection.

Claim 1 has been amended to recite: "...a second-stage inverter including: a first, P-type, transistor for driving a load at one of edges flank of the reference clock with which said clock synchronous circuit does not operate in synchronization; and a second, N-type, transistor for driving the load at the other edge flank of the reference clock with which said clock synchronous circuit operates in synchronization, the second transistor being formed to have a gate width equal or larger than a gate width of the first transistor..."

Amended Claim 1 clearly defines the relative dimensions of the P-type and N-type transistors. Specifically, The first transistor is a P-type and the second transistor is an N-type. The gate width of the second transistor is equal to or larger than the gate width of the first transistor. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claim 1 under 35 U.S.C. §112, second paragraph.

Claim 3 has been amended to recite: "The semiconductor integrated circuit device according to claim 1, wherein said first transistor has a gate width set to a gate width value that produces a change in the edge flank that is slowed down, the gate width value being selected so that a pulse waveform of the reference clock is not destroyed." (Emphasis added).

Amended Claim 3 clearly defines a range of gate width values for the first transistor as being bound by the requirements of producing a slowed down change in edge flank and not destroying the pulse waveform of the reference clock. Thus, any gate width value that meets both requirements is considered acceptable for the first transistor. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claim 3 under 35 U.S.C. §112, second paragraph.

II. Rejection of Claims 1-9 Under 35 U.S.C. §102(a)

Claims 1-9 have been rejected under 35 U.S.C. §102(a) as allegedly being anticipated by the admitted prior art as described in FIG. 7 of the application. Specifically, the prior art of FIG. 7 shows an inverter comprising a first 62 and second 61 transistor, where the second transistor 61 is of a different channel type than the first transistor 62 and the second transistor 61 has a gate width W_p that is larger than the first transistor's gate width W_n.

Amended Claim 1 specifically defines the first and second transistors recited as part of a second-stage inverter and that the relative dimensions of the second transistor to the first transistor is equal or larger. The second transistor is defined in amended Claim 1 as an N-type transistor, thus the transistor having the larger gap width is an N-type transistor and not a P-type transistor as disclosed in the admitted prior art shown in FIG. 7, thus obviating the §102 rejection. The changes to the limitations recited in Applicant's Claim 1 conform to the equation shown in FIG. 1, namely $W_p \leq W_n$. Therefore no new matter has been introduced by way of amended Claim 1. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claim 1 under 35 U.S.C. §102.

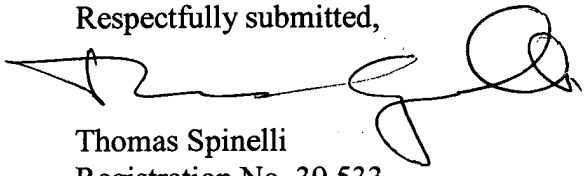
Claims 2-9 have been rejected under 35 U.S.C. §102 by virtue of their dependence from independent Claim 1, therefore, for at least the reasons given above in support of Claim 1, Claims 2-9 are believed allowable over the admitted prior art. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claims 2-9 under 35 U.S.C. §102.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-9 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,



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